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Patent

Docket No. 492322017300

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Tetsuro ASANO et al.

Serial No.: 10/521,941

Filing Date: February 6, 2006

For: SEMICONDUCTOR DEVICE

Examiner: Not Yet Assigned

Group Art Unit: 2811

**INFORMATION DISCLOSURE
STATEMENT UNDER 37 C.F.R. § 1.97 & 1.98**

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

Pursuant to 37 C.F.R. § 1.97 and § 1.98, Applicants submit for consideration in the above-identified application the documents listed on the attached Form PTO/SB/08a/b. Copies of the documents are also submitted herewith. The Examiner is requested to make these documents of record.

This Information Disclosure Statement is submitted before mailing of a first Office Action on the merits; accordingly, no fee or separate requirements are required.

Applicants would appreciate the Examiner initialing and returning the Form PTO/SB/08a/b, indicating that the information has been considered and made of record herein.

va-162306

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /JJ/

The information contained in this Information Disclosure Statement under 37 C.F.R. § 1.97 and § 1.98 is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to the examination of this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

In the unlikely event that the transmittal form is separated from this document and the Patent and Trademark Office determines that an extension and/or other relief (such as payment of a fee under 37 C.F.R. § 1.17 (p)) is required, Applicants petition for any required relief including extensions of time and authorize the Commissioner to charge the cost of such petition and/or other fees due in connection with the filing of this document to Deposit Account No. 03-1952 referencing (492322017300).

Dated: May 10, 2006

Respectfully submitted,

By 

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Substitute for form 1449/PTO		Complete if Known	
		Application Number	10/521,941
		Filing Date	February 6, 2006
		First Named Inventor	Tetsuro ASANO
		Art Unit	2811
		Examiner Name	Not Yet Assigned
		Attorney Docket Number	492322017300
(Use as many sheets as necessary)			
Sheet	1	of	1

U.S. PATENT DOCUMENTS				
Examiner Initials*	Cite No. ¹	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
				Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS				
Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
1.	JP-2-162744	06-22-1990		Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
2.	WO-97/45877	04-12-1997		Translation of abstract only

*EXAMINER: Initial if information considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTC Patent Documents at www.uspto.gov or MPEP 801.04. ³Enter Office that issued the document, by the two-letter code (Wipo Standard ST-3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WPO Standard ST-16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

NON PATENT LITERATURE DOCUMENTS				
Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		
3	MIYAWAKI, Yasuo et al. (1986) "Ion-Implanted Low Noise Dual-Gate GaAs MESFET," Sanyo Technical Review 18(2), pp. 76-84			

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Examiner Signature	/Jerome Jackson Jr. (10/01/2008)	Date Considered
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